said communication controller for controlling the exchange of data between a first one of said one or more processor chips and said other of said one or more processor chips;

wherein said computer processing architecture can be scaled larger by connecting together two or more of said processor chips in parallel via said I/O links of said processor chips, so as to create multiple processing core pipelines which share data therebetween.

20. The computer processing architecture as recited in claim 19, wherein one of said Q-number of registers in at least one of said one or more register files is a zero register which always stores zero.

21. The computer processing architecture as recited in claim 19, wherein program jumps are executed by adding a value to the current program counter value stored in the program counter register using a standard add operation.

22. The processing core as recited in claim 19, wherein memory addresses are calculated by adding a value to the current program counter value stored in the program counter register using a standard add operation.

23. The computer processing architecture as recited in claim 19, wherein program jump tables hold values, which are offset values from the current program counter value.

24. The computer processing architecture as recited in claim 19, wherein a processing instruction comprises N-number of P-bit instructions appended together to form a very long instruction word (VLIW), and said N-number of processing paths process N-number of P-bit instructions in parallel.

25. The computer processing architecture as recited in claim 24, wherein M=64, Q=64, and P=32.

26. The computer processing architecture as recited in claim 19, wherein said Q-number of registers within each of said one or more register files are either private or global registers, and wherein when a value is written to one of said Q-number of said registers which is a global register within one of said plurality of register files, said value is